

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert Pechman (RN: 45,002) and Robert J. Crawford (RN: 32,122) on September 11, 2008.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently amended) A down converter, comprising:

an integrated circuit having a control Field Effect Transistor (FET) (CF) disposed in a first well having a first polarity; and

a synchronous rectifier FET (SF) having a source region and a channel region both disposed in a second well having a second polarity opposite the first polarity,

wherein the control FET is a Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS) type and the SF is a vertical Metal Oxide Semiconductor type; the first and second wells are formed in contact with a heavily doped region of a substrate; and a conductivity-type of the LDMOS FET and a conductivity-type of a the heavily doped region of the substrate are of the same type;

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wherein at least a portion of the heavily doped region forms a drain region for the SF; and a source contact of the CF is connected to drain region of the SF via a conductive plug in the substrate.

2. (Previously presented) A down converter as recited in claim 1, wherein the synchronous rectifier FET is a Vertical Double-Diffused Metal Oxide Semiconductor (VDMOS) FET.

3. (Original) A down converter as recited in claim 1, wherein the synchronous rectifier FET is a vertical trench DMOS FET.

4-7. (Currently Cancelled)

8-9. (Cancelled)

10. (Original) A down converter as recited in claim 1, wherein the integrated circuit does not include isolation regions between the CF and the SF.

11. (Currently Amended) A down converter as recited in claim 1, wherein the conductivity type of the heavily doped region is n-type.

12. (Currently Cancelled)

13-20. (Cancelled).

21. (Previously Presented) A down converter as recited in claim 1, wherein the integrated circuit further includes one or more additional FETs configured to control gate switching of the control FET and the synchronous rectifier FET.

22. (Currently Amended) A down converter as recited in claim 1 further comprising an inductor, wherein a- the source contact of the control FET and a drain contact of the synchronous rectifier FET are connected to the inductor of the down converter.

23. (Currently Amended) A down converter as recited in claim 1 further comprising an inductor, wherein a- the source contact of the control FET and a drain contact of the synchronous rectifier FET are connected to the inductor of the down converter, the conductive plug ~~source contact of the control FET and the drain contact of the synchronous rectifier FET further having~~ forms a low-ohmic connections- to mitigate resistive and inductive parasitics of the integrated circuit.

24. (Previously Presented) A down converter as recited in claim 23, wherein the integrated circuit has a parasitic inductance on the order of 1 nH or less.

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25. (Currently Amended) A down converter as recited in claim 1 further including a voltage input, wherein the control FET has a drain contact connected to the voltage input of the down converter ~~and the control FET has a source contact connected to a drain contact of the synchronous rectifier FET.~~

26. (Currently Amended) A down converter as recited in claim 25, wherein the source contact of the control FET is connected to the drain contact of the synchronous rectifier FET via ~~a~~ the conductive plug and a portion of the heavily doped region in the substrate.

27. (Previously Presented) A down converter as recited in claim 1 wherein the control FET includes a gate driven by a control block supplied by an external capacitor.

Allowable Subject Matter

Claims 1-3, 10, 11 and 21-27 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811